OCM240128-9 图形点阵液晶显示模块

使用说明书

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上海思先电子有限公司

Shanghai Sixian Electronics Co; Ltd.

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1、 产品简介

主要工艺：COG
显示内容：240X128 点阵
显示模式：STN，POSITIVE
驱动条件：1/128Duty,1/12Bias
视向：6：00
背光：LED，白色
工作温度：-20℃-+70℃
储存温度：-30℃-+80℃
驱动 IC：UC1608

2、 引用文件

UC1608 规格书

3、机械特性

类别	标准值	单位
模块	131.5（w）X91.00(h)X9.2(t)Max	mm
有效显示区	112.0(w)X62.0(h)	mm
点大小	0.4(w)X0.4(h)	mm
点间隙	0.05(w)X0.05(h)	mm

4、光电特性

类别	符号	条件	最小值	TYP	最大值	单位
驱动电压	Vop.	25℃	8.8	9.0	14.5	V
响应时间	Ton	25℃	—	127	400	Ms
对比度	Toff	25℃	—	263	400	Ms
	CR	25℃	—	9	—	—
视角范围		25℃	—	88	—	DEG
交叉效应		25℃	—	1.2	—	—

5、极限参数

参数	符号	最小值	最大值	单位
逻辑电压	Vdd	-0.3	+3.30	V
驱动电压	Vout,VO	-0.3	+14.5	V
工作温度	Top	-20	+70	℃
存储温度	Tst	-30	+80	℃

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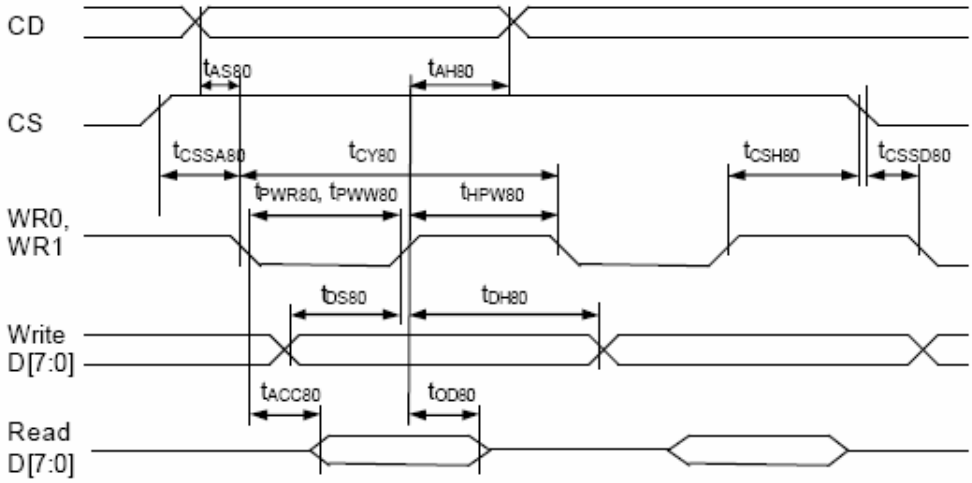
6、接口时序

AC CHARACTERISTICS



(2.7V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 20	–	nS
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 140 140 140	–	nS
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 65	–	nS
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	–	nS
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 12	60 20	nS
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS

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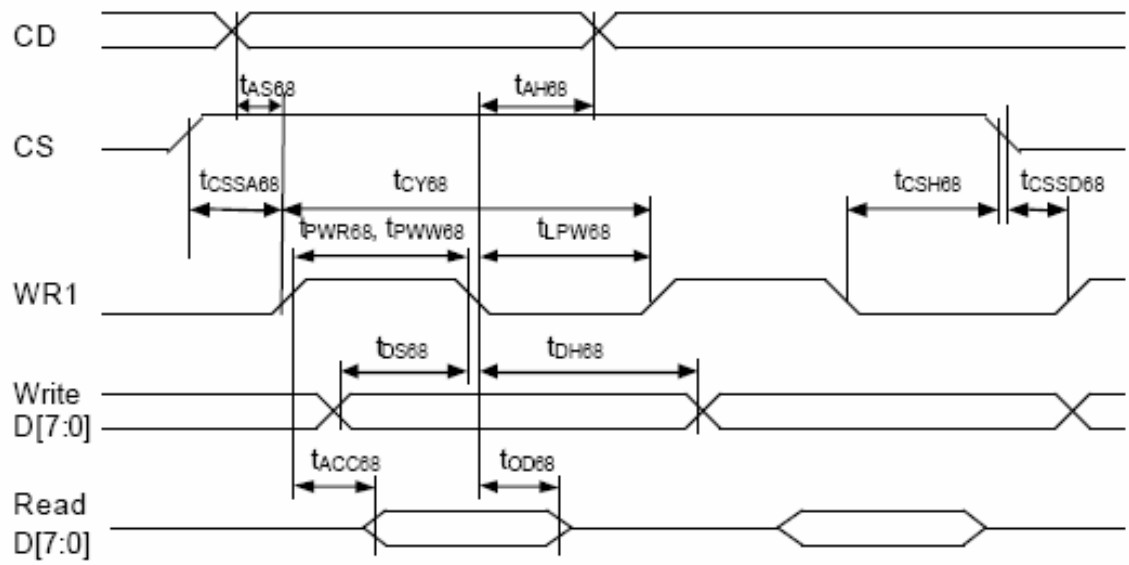

(2.7V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	nS
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 140 140 140	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 65	– 	 nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 12	60 20	nS
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

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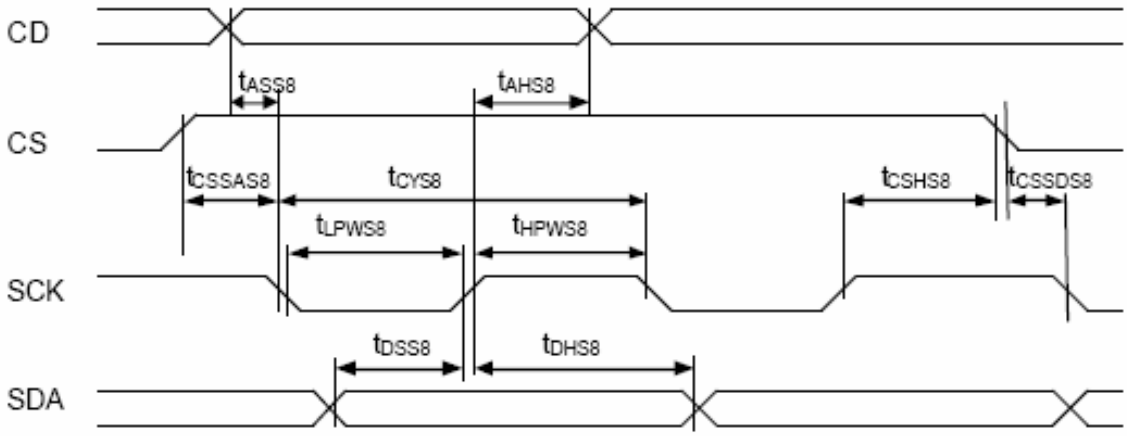
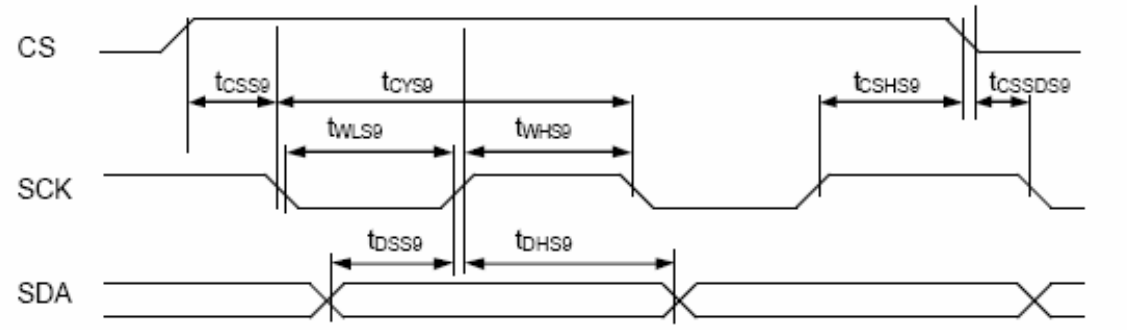


(2.7V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		20	–	nS
t_{CYS8}	SCK	System cycle time		140	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS	Chip select setup time		10 20 10		nS



(2.7V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		140	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS	Chip select setup time		10 20 10		nS

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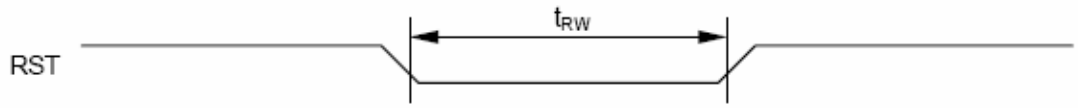

(2.7V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1000	–	nS

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7、直流特性（VDD=2.84V）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.7	2.8	3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8	3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq 2.7V, 25^{O}C$		12.5	16	V
V_D	LCD data voltage	$V_{DD2/3} \geq 2.7V, 25^{O}C$			1.53	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 12.5V		1.5	3	k O
$R_{0(COM)}$	COM output impedance	V_{LCD} = 9		1.5	3	k O
f_{LINE}	Average frame rate		69	75	--	Hz

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8、引脚描述

接口定义：

引脚编号	引脚名称	方向	引脚功能描述
1	VSS	I	逻辑电源地 0V
2	VDD	I	逻辑电源正 3.3V
3	CS	I	片选信号，H 有效
4	C/D	-	数据\指令选择：高电平：DB0-DB7 为显示数据 低电平：DB0-DB7 为操作指令
5	WR0	I	当接口定义为 6800 接口时，读/写控制脚：RW=H：读操作 RW=L：写操作 当接口定义为 8080 接口时，/WR 为写入控制脚
6	WR1	I	当接口定义为 6800 接口时，为使能控制脚，E=H 有效 当接口定义为 8080 接口时，/RD 为读控制脚，低有效
7	DB0	I/O	数据输入输出引脚
8	DB1	I/O	数据输入输出引脚
9	DB2	I/O	数据输入输出引脚
10	DB3	I/O	数据输入输出引脚
11	DB4	I/O	数据输入输出引脚
12	DB5	I/O	数据输入输出引脚
13	DB6	I/O	数据输入输出引脚
14	DB7	I/O	数据输入输出引脚
15	G/CS	I	片选输入，低有效（辅助 IC）
16	G-SO	-	串行数据输出（辅助 IC）
17	G-SI	-	串行数据输入（辅助 IC）
18	SCLK	-	串行时钟输入（辅助 IC）
19	LED+	I	背光电源,LED+（3.3V）
20	LED-	I	背光电源,LED-（0V）

注： 辅助字库IC 的应用可以参考《标准汉字字库芯片使用手册》，在公司网站可以下载

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9、命令描述

指令表：

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Mux Rate and temperature compensation.	0	0	0	0	1	0	0	#	#	#	Set {MR, TC[1:0]}	MR: 1b TC: 00b
6	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	101b
7	Set Adv. Program Control. (double byte command)	0	0	0	0	1	1	0	0	0	R	For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
8	Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9	Set Gain and Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set {GN[1:0], PM[5:0]}	GN=3 PM=0
		0	0	#	#	#	#	#	#	#	#		
10	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
11	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0=disable
12	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0=disable
13	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0=disable
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
16	Set LCD Mapping Control	0	0	1	1	0	0	#	#	#	#	Set LC[3:0]	0
17	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
18	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
19	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b=12
20	Reset Cursor Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
21	Set Cursor Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
22	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		

指令介绍：

(1) Write data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) Read data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1,2) operations access display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will be incremented automatically depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 15), PA will be wrapped around to the other end of RAM and continue.

(3) Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1

Status flag definitions:

BZ: Busy with internal process.
MX: Status of register LC[2], mirror X.
DE: Display enable flag. DE=1 when display enabled
RS: Reset in progress. If RS=1, host interface will be inaccessible.
WA: status of register AC[0]. Automatic column/page wrap around.
GN0, 1: GN[1:0]. register Gain

(4) Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	0	0	0	1	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA possible value=0-239

(5) Set Multiplex Rate and Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Multiplex Rate MR Set Temperature Compensation TC[1:0]	0	0	0	0	1	0	0	MR	TC1	TC0

Set the multiplex ratio (number of rows) and temperature compensation.

MUX ratio definition: 0b=96 1b=128

Temperature compensation curve definition:

00b= -0.00%/C 01b= -0.05%/C 10b= -0.10%/C 11b= -0.20%/C

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(6) Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[2:0]	0	0	0	0	1	0	1	PC2	PC1	PC0

Set PC[1:0], according to the capacitance loading of LCD panel.

Panel loading definition:

00b: LCD < 26 nF **01b: 26 nF < LCD < 43 nF**

10b: 43 nF < LCD < 60nF 11b: 60nF < LCD < 90 nF

Set PC[2] to program to use internal charge pump of external V_{LCD} source.

Pump control definition:

0b=External V_{LCD} **1b=Internal V_{LCD}**

(7) Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[0] (Double byte command)	0	0	0	0	1	1	0	0	0	R
	0	0	APC register parameter							

For UltraChip only. Please Do NOT use.

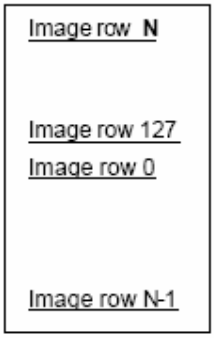
(8) Set Start Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Start Line SL[5:0]	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0

Set the start line number

Start line setting will scroll the displayed image up by SL rows. The valid value is between 0 (no scrolling) and 63. One example of the visual effect on LCD is illustrated in the figure below.

SL=0



SL=N

(9) Set Gain and Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gain and Potentiometer	0	0	1	0	0	0	0	0	0	1
GN [1:0] PM [5:0] (Double byte command)	0	0	GN1	GN0	PM5	PM4	PM3	PM2	PM1	PM0

Program Gain (GN[1:0]) and Potentiometer (PM[5:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range of GN = 0 ~ 3 PM value = 0 ~ 63

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(10) Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0] - WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1] – Reserved (always set to 0)

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
When WA=1, controls whether page address will be adjusted by +1 or -1, when CA reached CA boundary.
No effect when WA=0.

CA boundary is 239 and PA boundary is 15 when PID=0, PA boundary is 0 when PID=1.

(11) Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel On DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(12) Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data stored in display memory. This function has no effect on the existing data stored in display RAM.

(13) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	1	0	1	0	1	1	1	DC2

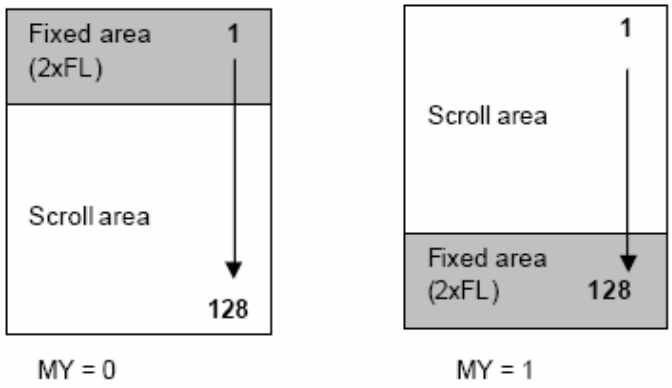
This command is for programming registers DC[2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1608 will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

(14) Set Fixed Lines

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	1	0	0	1	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

(15) Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	1	0	1	1	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface.
Effective range of value = 0 ~ 15

(16) Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[3:0]	0	0	1	1	0	0	MY	MX	0	MSF

Set LC[3:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 239-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

MSF is implemented by MSB-LSB swapping. When MSB first (LC[0]) bit is set, data D[7:0] will be re-aligned as D[0:7] then be stored to RAM.

(17) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. The system will take about 15ms to reset

(18) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

(19) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b= 10.7 01b=11.3 **10b=12.0** 11b=12.7

(20) Reset Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Return to Cursor. AC[3]=0, CA=CR	0	0	1	1	1	0	1	1	1	0

This command is used to reset cursor update mode function. See description below.

(21) Set Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	1	1	1	0	1	1	1	1

Set Cursor Mode command is used to turn on cursor update mode function. AC[3] will be set to 1, register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increment with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support " Read-Modify-Write" for cursor implementation.

Reset Cursor Mode command will clear cursor update mode flag (AC[3]=0), CA will be restored to previous CA value which is stored in CR, and CA, PA increment will return to its normal condition.

(22) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	1	1	1	0	0	1	TT	
	0	0	Testing parameter							

This command is used for UltraChip production testing. For UltraChip Only. Please do not use.

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11、附录

初始化程序参考：

```
//.....初始化.....
void lcm_init(void)
{
    lcm_cs=0;
    lcm_wr1=0;
    delay_n_ms(20);
    send_cmd(0xE2);//Software Reset
    delay_n_ms(20);
    send_cmd(0x25);//Set Multiplex Rate and Temperature Compensation
    send_cmd(0xEA);//Set LCD Bias Ratio(1/12 bias)
    send_cmd(0x81);//Set Gain and Potentiometer
    send_cmd(0x88);//Set Gain and Potentiometer
    send_cmd(0x2C);//Set Power Control
    send_cmd(0x8D);
    send_cmd(0xC0);

    send_cmd(0x40);//Set Start Line
    send_cmd(0xAF);//Set Display On
}
```

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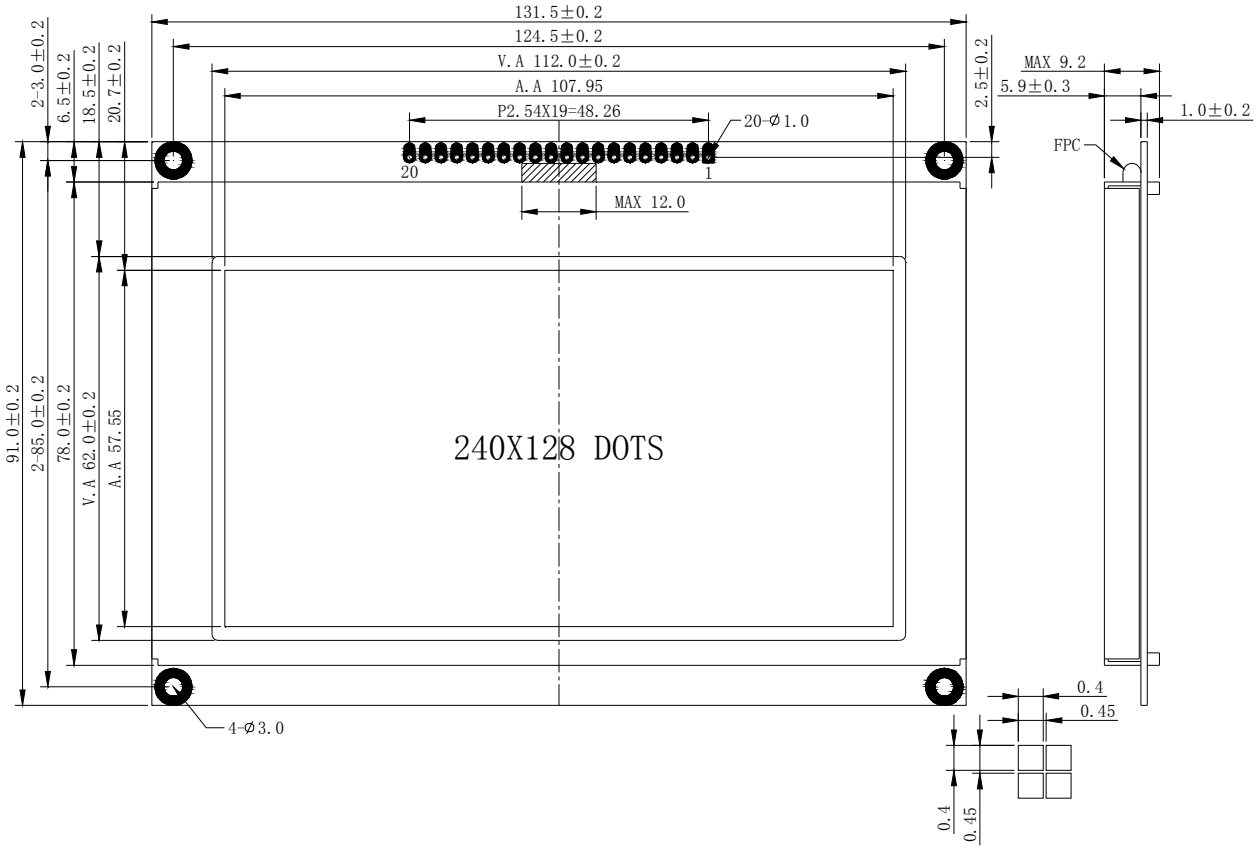
模块外形图



J1 接口定义

1	2	3	4	5	6	7	8	9	10
VSS	VDD	CS	C/D	WR0	WR1	DB0	DB1	DB2	DB3
11	12	13	14	15	16	17	18	19	20
DB4	DB5	DB6	DB7	G/CS	G-S0	G-S1	SCLK	LED+	LED-

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