OCM128128-4 图形点阵液晶显示模块

使用说明书

感谢您关注和使用我们的液晶显示器产品， 欢迎您提出您的要求、意见和建议，我们将竭诚为您服务、让您满意。您可以浏览 www.shsixian.com了解最新的产品与应用信息,或拨打热线电话 021-53083613 以及向sx@shsixian.com 邮箱发 E-mail 获取具体的技术咨询与服务

上海思先电子有限公司

Shanghai Sixian Electronics Co; Ltd.

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1、 产品简介

主要工艺：COG
显示内容：128X128 点阵
显示模式：STN/FSTN，POSITIVE
驱动条件：1/128Duty,1/9Bias
视角：6：00
背光：LED，白色
工作温度：-20℃-+70℃
储存温度：-30℃-+80℃
驱动 IC：UC1617S

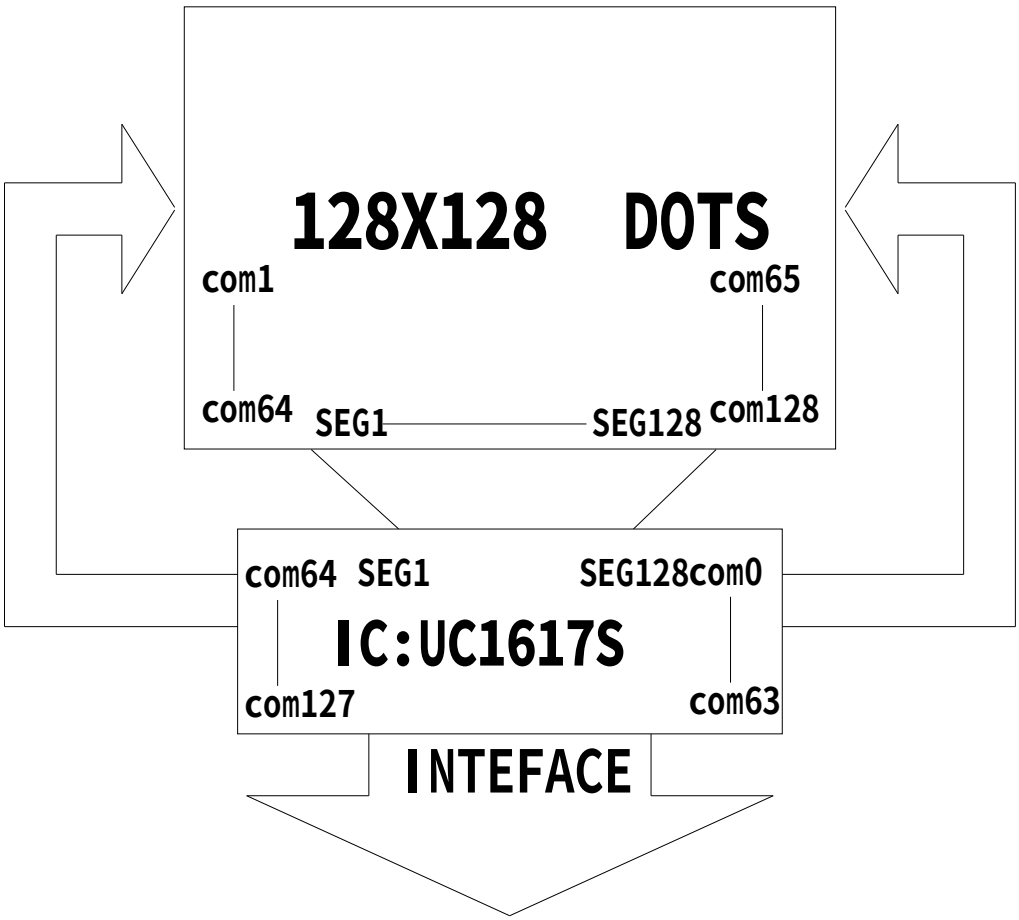
2、 引用文件

UC1617S 规格书

3、机械特性

类别	标准值	单位
模块	91.0（w）X91.0(h)X10.7(t)	mm
有效显示区	65.8(w) X 58.8(h)	mm
点大小	0.463(w) X 0.4083(h)	mm
点间隙	0.02(w) X 0.02(h)	mm

4、产品框图



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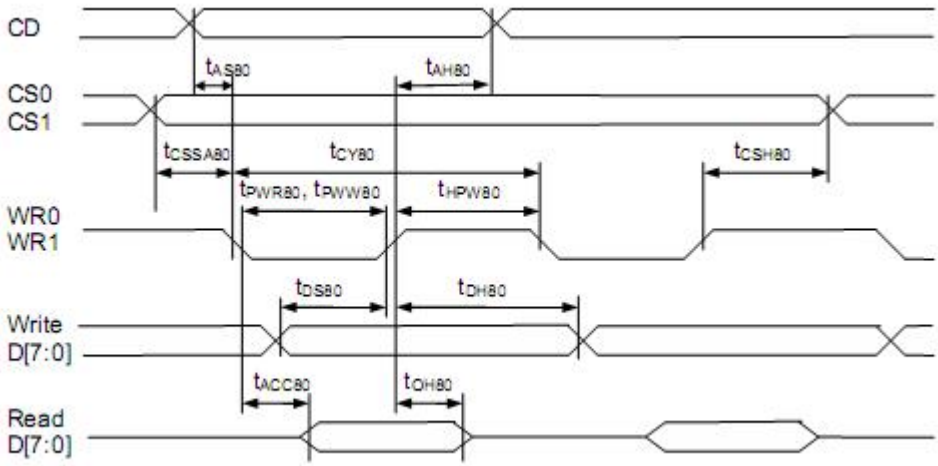
5、光电特性

类别	符号	条件	最小值	TYP	最大值	单位
驱动电压	Vop.	25℃	8.8	12.5	18.0	V
响应时间	Ton	25℃	—	127	400	Ms
对比度	Toff	25℃	—	263	400	Ms
	CR	25℃	—	9	—	—
视角范围		25℃	—	88	—	DEG
交叉效应		25℃	—	1.2	—	—

6、极限参数

参数	符号	最小值	最大值	单位
逻辑电压	Vdd	-0.3	+4.0	V
驱动电压	Vout,VO	-0.3	+4.0	V
工作温度	Top	-20	+70	℃
存储温度	Tst	-30	+80	℃

7、接口时序



(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		170 130	–	nS
t_{PWR80}	WR1	Pulse width (read)		85	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		85 65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	65 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

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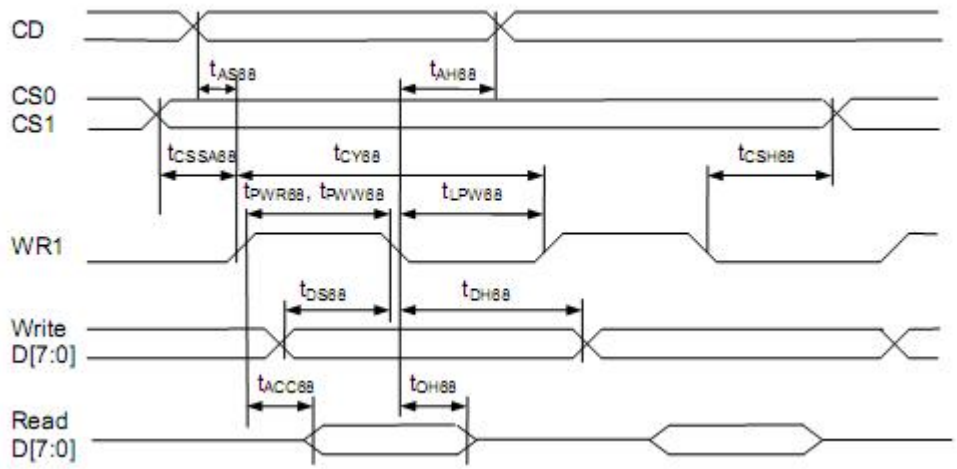

(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS88} t_{AH88}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY88}		System cycle time (read) (write)		170 130	–	nS
t_{PWR88}	WR1	Pulse width (read)		85	–	nS
t_{PWW88}		Pulse width (write)		65	–	nS
t_{LPW88}		Low pulse width (read) (write)		85 65	–	nS
t_{DS88} t_{DH88}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC88} t_{OH88}		Read access time Output disable time	C_L = 100pF	– –	70 30	nS
t_{CSSA88} t_{CSH88}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS88} t_{AH88}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY88}		System cycle time (read) (write)		320 270	–	nS
t_{PWR88}	WR1	Pulse width (read)		160	–	nS
t_{PWW88}		Pulse width (write)		135	–	nS
t_{LPW88}		Low pulse width (read) (write)		160 135	–	nS
t_{DS88} t_{DH88}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC88} t_{OH88}		Read access time Output disable time	C_L = 100pF	– –	120 60	nS
t_{CSSA88} t_{CSH88}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

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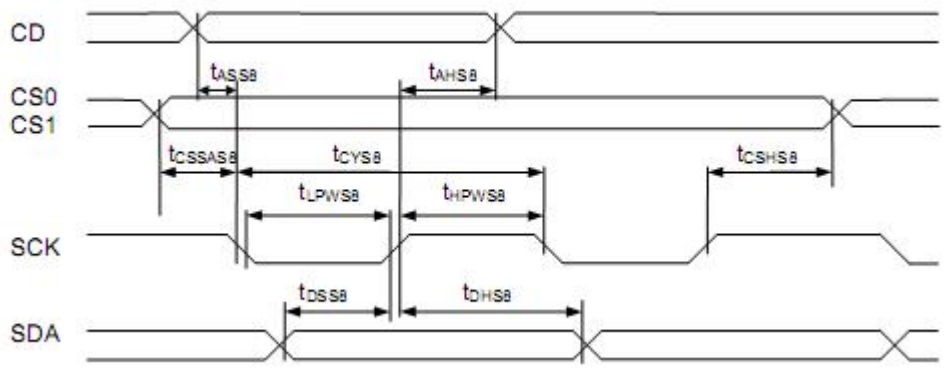

(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		35	–	nS
t_{LPWS8}		Low pulse width		17	–	nS
t_{HPWS8}		High pulse width		17	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 5	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS
Read:						
t_{CYS8}	SCK	System cycle time		110	–	nS
t_{LPWS8}		Low pulse width		55	–	nS
t_{HPWS8}		High pulse width		55	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time	C_L = 100pF	– N/A	50 N/A	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		60	–	nS
t_{LPWS8}		Low pulse width		30	–	nS
t_{HPWS8}		High pulse width		30	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		24 5	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS
Read:						
t_{CYS8}	SCK	System cycle time		185	–	nS
t_{LPWS8}		Low pulse width		92	–	nS
t_{HPWS8}		High pulse width		92	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time	C_L = 100pF	– N/A	90 N/A	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

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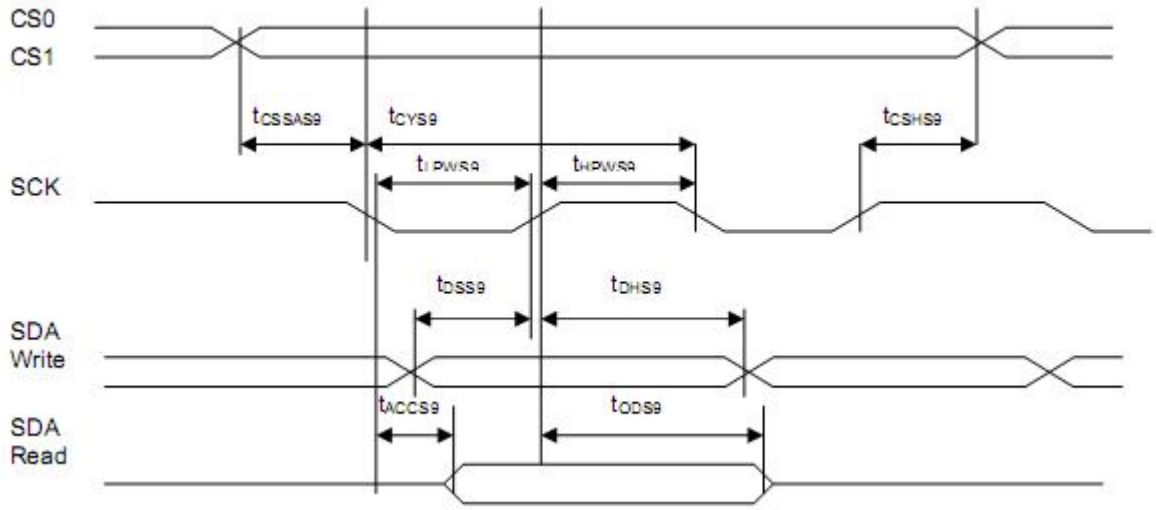

(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{CYS9}	SCK	System cycle time		35	–	nS
t_{LPWS9}		Low pulse width		17	–	nS
t_{HPWS9}		High pulse width		17	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 5	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS
Read:						
t_{CYS9}	SCK	System cycle time		110	–	nS
t_{LPWS9}		Low pulse width		55	–	nS
t_{HPWS9}		High pulse width		55	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time	C_L = 100pF	– N/A	50 N/A	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
Write :						
t_{CYS9}	SCK	System cycle time		60	–	nS
t_{LPWS9}		Low pulse width		30	–	nS
t_{HPWS9}		High pulse width		30	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		24 5	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS
Read:						
t_{CYS9}	SCK	System cycle time		185	–	nS
t_{LPWS9}		Low pulse width		92	–	nS
t_{HPWS9}		High pulse width		92	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time	C_L = 100pF	– N/A	90 N/A	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

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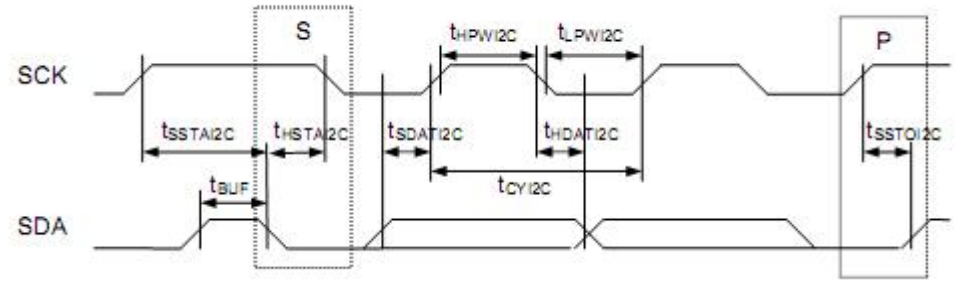
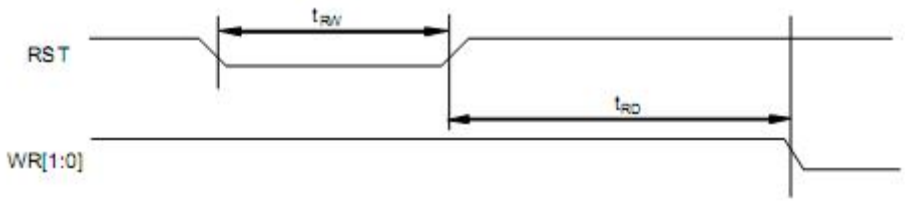


(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ≤ 100nS	580 275	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		290 137	–	nS
t_{HPWI2C}		High pulse width (read) (write)		290 137	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		28	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		28	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		165	–	nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ≤ 100nS	750 330	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		375 165	–	nS
t_{HPWI2C}		High pulse width (read) (write)		375 165	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		55	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		60	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		220		nS



(1.65V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

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8、直流特性（VDD=2.84V）

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.6		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ ≥ 2.6V, 25°C		14	15	V
V_D	LCD data voltage	$V_{DD2/3}$ ≥ 2.6V, 25°C	0.89		1.78	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85°C			50	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ONS(COM)}$	Downward COM output impedance			1.85	2.5	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	21.1	+10%	kHz

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 14 V,
Mux Rate = 128,
C_B = 2.2 μF,
All HV outputs are open circuit.

Bias Ratio = 11,
Line Rate = 00 b,
Bus mode = 6800,
Temperature = 25°C,

PM = 78,
Panel Loading (PC[1:0]) = 10b,
C_L = 330 nF,
MTP = 00 H,

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	435	653
2-pixel checker	Bus = idle	462	693
-	Reset (standby current)	< 1	5

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9、引脚描述

接口定义：

引脚编号	引脚名称	方向	引脚功能描述
1	VSS	-	逻辑电源地（0V）
2	VDD	-	逻辑电源正
3	RES	0	复位信号，低电平有效
4	CS0	0	片选择信号，L：选通
5	CD	0	命令/数据
6	WR0	0	WR[1:0]控制器读/写接口，详见主机接口部说明。当并行模式时,WR[1:0]是 6800/8080 模式间的选择，当串行模式时，这两个引脚不使用，请连接到 VSS。
7	WR1	0	
8	D0	I/O	数据输入输出引脚 0
9	D1	I/O	数据输入输出引脚 1
10	D2	I/O	数据输入输出引脚 2
11	D3	I/O	数据输入输出引脚 3
12	D4	I/O	数据输入输出引脚 4
13	D5	I/O	数据输入输出引脚 5
14	D6	I/O	数据输入输出引脚 6
15	D7	I/O	数据输入输出引脚 7
16	NC	0	悬空
17	A	I/O	背光电源正
18	K	I/O	背光电源负
19	SO	I	串行数据输出（辅助 IC）
20	/CS	I	显示片选信号（低有效）
21	SCK	I/O	串行时钟输入
22	SI	I	串行数据输入（辅助 IC）

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10、命令描述

指令表：

The following is a list of host commands supported by UC1617s

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	-	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Prod_Code, PID}	N/A
				Ver	PMO[5:0]								
				Prod_Code				0	PID	0	0		
4.	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	00H
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8.	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1 or 2	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10.	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0H
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0H
11.	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	4EH
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
12.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[10:9]	00b: Disable
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	00H
				#	#	#	#	#	#	#	#		
15.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18.	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[3:0]	6H
				–	–	–	–	#	#	#	#		
21.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	01b
22.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[8:7]	10b
23.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25.	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
27.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
30.	Set Window Program Starting Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	0 #	0 #	Shared with MTP commands	Set WPC0	0
31.	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
32.	Set Window Programming Ending Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	1 #	0 #		Set WPC1	31
33.	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
34.	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Disable
35.	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
36.	Set MTP Write Mask	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[5:0]		0
37.	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
38.	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	
39.	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	
40.	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	
SERIAL READ COMMAND (ENABLED ONLY IN S8/S9 MODE)														
41.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status until chip disabled		N/A
		0	1	-	MX	MY	WA	DE	WS	MD	MS			
		0	1	Ver			PMO[5:0]							
		0	1	Prod Code				0	PID	0	0			

Notes:

- Any bit patterns other than the commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on register MTPC[3].
- Commands (37)~(40) are shared with commands (30)~(33) and have exactly the same code. When MTPC[3]=0, commands (37)~(40) are interpreted as `Window Programming` commands. When MTPC[3]=1, they are the `MTP Control` commands.
- MTPM and PM are actually the same register. Only one of the commands (36 or 11) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.

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指令介绍

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Row Address register (RA) and Page_C Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each page_c of pixel corresponds to one page_c of SRAM data. RA and CA registers can be programmed by issuing `Set row Address` and `Set Page_C Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of page_c address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (PID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 31), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	-	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]	PMO[5:0]						
			Product Code				0	PID	0	0

Status 1 definitions:
- *MX*: Status of register LC[1], mirror X.
- *MY*: Status of register LC[2], mirror Y.
- *WA*: Status of register AC[0]. Automatic page_c/row wrap around.
- *DE*: Display enable flag. DE=1 when display is enabled
- *WS*: MTP Command Succeeded
- *MD*: MTP Option (1 - MTP version, 0 - non-MTP version)
- *MS*: MTP action status

Status 2 definitions:
- *Ver[1:0]*: IC Version Code, 00 ~ 11. Default: 00
- *PMO[5:0]*: PM offset value

Status 3 definitions:
- *Prod_Code*: 0111b (7h)
- *PID*: Provide connection status of accessing to ID pin.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page_C Address LSB CA[4:0]	0	0	0	0	0	CA4	CA3	CA2	CA1	CA0

Set SRAM page_c address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~31

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(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.00%/°C 01b= -0.10%/°C 10b= -0.15%/°C 11b= -0.05%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b≤6nF 01b=6~9nF **10b=9~13nF** 11b=13~18nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	0	0	1	0	1	1	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External V_{LCD} **11b= Internal V_{LCD}** (9X pump, standard)

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R]	0	0	0	0	1	1	0	0	R	R
(Double-byte command)	0	0	APC register parameter							

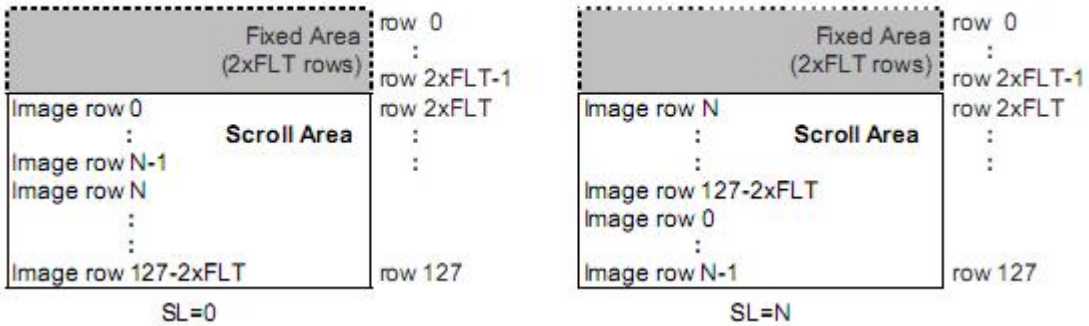
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	0	1	0	1	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by `Set Fixed Lines` command.



(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address RA [3:0]	0	0	0	1	1	0	RA3	RA2	RA1	RA0
Set Row Address RA [6:4]	0	0	0	1	1	1	-	RA6	RA5	RA4

Set SRAM row Address for read/write access.

Possible value = 0~127

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	1	0	0	0	0	0	0	1
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 193**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [10:9]	0	0	1	0	0	0	0	1	LC10	LC9

This command is used to enable partial display function.

LC[10:9] : **0xb: Disable Partial Display**, Mux-Rate = CEN+1 (DST, DEN not used.)
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic page_c/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increase by one.

AC[1]: Auto-Increment order
0 : page_c (CA) increase (+1) first until CA reaches CA boundary, then RA will increase by (+/-1).
1 : row (RA) increase (+/-1) first until RA reach RA boundary, then CA will increase by (+1).

AC[2]: RID, Row Address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether row Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[3]=ON), see Command Description (31) ~ (35) for more details. When Window Program is disabled (AC[3]=OFF), the behavior of CA, RA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[3]=ON.

(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	1	0	0	1	0	0	0	0
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.

MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ≥ FLTx2
DEN ≤ (CEN-FLBx2).

MY=1 DST ≥ FLBx2
DEN ≤ (CEN-FLTx2)

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate * Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 85, 64, 43, and 32.
The followings are line rates at Mux Rate = 86~128:

00b: 14.2 Klps 01b: 17.3 Klps 10b: 21.1 Klps 11b: 25.7 Klps
(Klps: Kilo-Line-per-second)

while the followings are line rates in On/Off mode:

00b: 5.7 Klps 01b: 7.0 Klps 10b: 8.5 Klps 11b: 10.4 Klps

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(18) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	1	0	1	0	1	1	DC3	DC2

This command is for programming register DC[3:2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit, and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1617s will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3]: Gray Shade and B/W mode
0b: B/W Mode **1b: 4-Shade Mode**

For B/W mode, use data format for 4-shade-mode and UC1617s will convert them for B/W mode automatically.

Note : When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1617s for 5~10mS after setting DC[2] to 1.

(19) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for programming LC[2:0] for COM (row) mirror (MY), SEG (page_c) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 31-CA as write/read (from host interface) display RAM page_c address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

(20) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [3:0]	0	0	1	1	0	0	1	0	0	0
(Double-byte command)	0	0	-	-	-	-	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[5:0] for N-Line Inversion:

NIV[1:0]: 00b: 9 lines 01b: 13 lines
10b: 17 lines 11b: 23 lines
NIV[2]: 0b: no-XOR **1b: XOR**
NIV[3]: **0b: Disable NIV** 1b: Enable NIV

(21) SET LCD GRAY SHADE 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[6:5]	0	0	1	1	0	1	0	0	LC6	LC5

This command sets gray scale register (LC[6:5]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[6:5]: Select Gray-shade
00b: 1 **01b: 2** 10b: 3 11b: 4

LC[6:5]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	1	9
01b	2	12
10b	3	15
11b	4	21

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(22) SET LCD GRAY SHADE 2

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[8:7]	0	0	1	1	0	1	0	1	LC8	LC7

This command sets gray scale register (LC[8:7]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[8:7]: Select Gray-shade
00b: 3 01b: 4 **10b: 5** 11b: 6

LC[8:7]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	3	15
01b	4	21
10b	5	24
11b	6	27

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:
00b = 6 01b = 9 10b = 10 **11b = 11**

***(27)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	1	1	1	1	0	0	0	1
(double-byte command)	0	0	-	*CEN [6:0]* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

***(28)* SET DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	1	1	1	1	0	0	1	0
(double-byte command)	0	0	-	*DST [6:0]* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

***(29)* SET DISPLAY END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	1	1	1	1	0	0	1	1
(double-byte command)	0	0	-	*DEN [6:0]* register parameter						

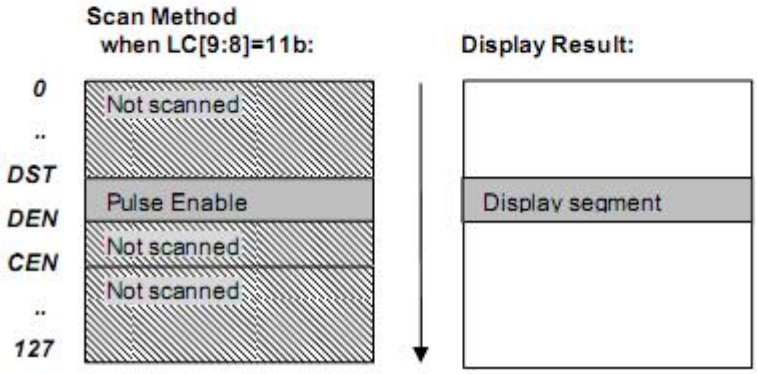
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

CEN, DST DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9:8]=11b, the Mux-Rate is narrowed down to DST-DEN+1 + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use B/W mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(30) SET WINDOW PROGRAM STARTING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (double-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	-	-	-	*WPC0[4:0]* register parameter				

This command is to program the starting page_c address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	-	*WPP0[6:0]* register parameter						

This command is to program the starting row Address of RAM program window.

(32) SET WINDOW PROGRAM ENDING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	-	-	-	*WPC1[4:0]* register parameter				

This command is to program the ending page_c address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (double-byte command)	0	0	1	1	1	1	0	1	1	1
	0	0	-	*WPP1[6:0]* register parameter						

This command is to program the ending row Address of RAM program window.

(34) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	1	1	1	1	1	0	0	AC3

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]) , PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row / page_c after reaching the specified window page_c / row boundary. PID controls the RAM address increasing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM page_c address increasing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

(35) SET MTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (double-byte command)	0	0	1	0	1	1	1	0	0	0
	0	0	-	-	*MTPC* register parameter					

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)
MTPC[5] : For testing only. Set to 0 for normal operation.

The following commands (36~40) are only valid when MTPC[3] =1:

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(36) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (double-byte command)	0	0	1	0	1	1	1	0	0	1
	0	0	-	-	*MTPM[5:0]* register parameter					

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0]: Set PMO value

This command is only valid when MTPC[3]=1.

(37) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (double-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	Shared register parameter							

This command is for fine tuning V_{MPT1} (use with BR=00) and is only valid when MTPC[3]=1.

(38) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} (use with BR=10) and is only valid when MTPC[3]=1.

(39) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(40) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (double-byte command)	0	0	1	1	1	1	0	1	1	1
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

Serial Read Command (Enable only in S8/S9 mode):

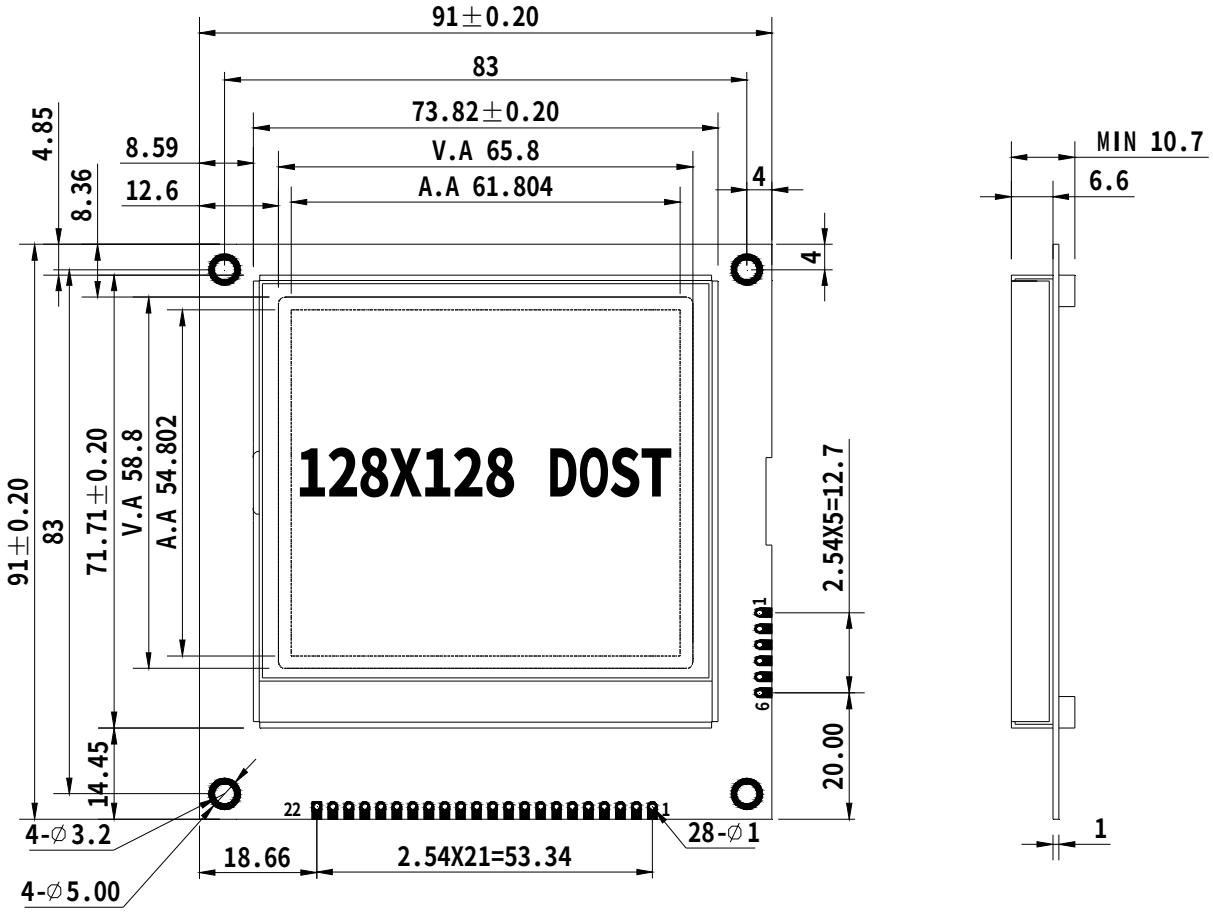
(41) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	1	1	1	1	1	1	1	0
	0	1	-	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]	PMO[5:0]						
			Prod_Code				0	PID	0	0

Please refer to command (3).

11、附录

模块外形图



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